CLAIMS:

1. A power amplifier comprising:

a transconductance stage that is operable to receive an input voltage signal and to produce an output current signal, the transconductance stage including a first Metal Oxide Silicon (MOS) transistor having a first gate oxide thickness and a first channel length;

a cascode stage communicatively coupled to the transconductance stage that is operable to receive the output current signal and to produce an output voltage signal based thereupon, the cascode stage including a second MOS transistor having a second gate oxide thickness and a second channel length; and

wherein the second gate oxide thickness is substantially thicker than the first gate oxide thickness.

2. The power amplifier of claim 1, wherein the second gate oxide thickness is approximately twice as thick as the first gate oxide thickness.

3. The power amplifier of claim 2, wherein:

the second gate oxide thickness is approximately 100 Angstroms; and

the first gate oxide thickness is approximately 50 Angstroms.

4. The power amplifier of claim 1, wherein the second channel length is substantially longer than the first channel length.

5. The power amplifier of claim 4, wherein the second channel length is approximately twice as long as the first channel length.

6. The power amplifier of claim 5, wherein:

the second channel length is approximately 0.35 microns; and

the first channel length is approximately 0.18 microns.

7. The power amplifier of claim 1, wherein:

the first MOS transistor includes a source tied to ground, a gate that receives the input voltage signal, and a drain; and

the second MOS transistor includes a source tied to the drain of the MOS transistor of the transconductance stage, a gate that receives a cascode bias voltage, and a drain; and

the power amplifier further comprises a circuit element having a first terminal coupled to a voltage supply and a second terminal coupled to the drain of the second MOS transistor.

8. The power amplifier of claim 1:

wherein the transconductance stage further includes an inductor having a first terminal coupled to a transconductance stage voltage supply and a second terminal tied to a drain of the first MOS transistor, wherein a source of the first MOS transistor couples to ground, and wherein a gate of the first MOS transistor receives the input voltage signal;

wherein the cascode stage includes:

a first inductor having a first terminal coupled to a cascode stage voltage supply and a second terminal coupled to a drain of the second MOS transistor;

a second inductor having a first terminal coupled to a source of the second MOS transistor and a second terminal coupled to ground; and

further comprising an AC coupling stage that couples the drain of the first MOS transistor that produces the output current signal to a gate of the second MOS transistor.

9. The power amplifier of claim 1, further comprising a signal level detection and bias determination module that is operable to apply a controllable bias voltage to the gate of the first MOS transistor.

10. The power amplifier of claim 1, further comprising a signal level detection and bias determination module that is operable to apply a controllable bias voltage to the gate of the second MOS transistor.

11. The power amplifier of claim 1, wherein the transconductance stage comprises:

a primary portion that receives the input voltage signal and that produces a primary output current signal;

a secondary portion that receives the input voltage signal and that produces a secondary output current signal; and

wherein the primary output current signal combines with the secondary output current signal to produce the output current signal.

12. The power amplifier of claim 11, wherein the primary portion and the secondary portion of the transconductance stage are operable to be biased at different levels.

13. A differential power amplifier comprising:

a pair of differential sides, each of the differential sides comprising:

a transconductance stage that is operable to receive an input voltage signal and to produce an output current signal, the transconductance stage including a first Metal Oxide Silicon (MOS) transistor having a first gate oxide thickness and a first channel length;

a cascode stage communicatively coupled to the transconductance stage that is operable to receive the output current signal and to produce an output voltage signal based thereupon, the cascode stage including a second MOS transistor having a second gate oxide thickness and a second channel length; and

wherein the second gate oxide thickness is substantially thicker than the first gate oxide thickness.

14. The power amplifier of claim 13, wherein the second gate oxide thickness is approximately twice as thick as the first gate oxide thickness.

15. The power amplifier of claim 14, wherein:

the second gate oxide thickness is approximately 100 Angstroms; and

the first gate oxide thickness is approximately 50 Angstroms.

16. The power amplifier of claim 13, wherein the second channel length is substantially longer than the first channel length.

17. The power amplifier of claim 16, wherein the second channel length is approximately twice as long as the first channel length.

18. The power amplifier of claim 17, wherein:

the second channel length is approximately 0.35 microns; and

the first channel length is approximately 0.18 microns.

19. The power amplifier of claim 13, wherein for each differential side:

the first MOS transistor includes a source tied to ground, a gate that receives the input voltage signal, and a drain; and

the second MOS transistor includes a source tied to the drain of the MOS transistor of the transconductance stage, a gate that receives a cascode bias voltage, and a drain; and

the power amplifier further comprises a circuit element having a first terminal coupled to a voltage supply and a second terminal coupled to the drain of the second MOS transistor.

20. The power amplifier of claim 13, wherein for each differential side:

the transconductance stage further includes an inductor having a first terminal coupled to a transconductance stage voltage supply and a second terminal tied to a drain of the first MOS transistor, wherein a source of the first MOS transistor couples to ground, and wherein a gate of the first MOS transistor receives the input voltage signal;

the cascode stage includes:

a first inductor having a first terminal coupled to a cascode stage voltage supply and a second terminal coupled to a drain of the second MOS transistor;

a second inductor having a first terminal coupled to a source of the second MOS transistor and a second terminal coupled to ground; and

the differential side further comprising an AC coupling stage that couples the drain of the first MOS transistor that produces the output current signal to a gate of the second MOS transistor.

21. The power amplifier of claim 13, further comprising a signal level detection and bias determination module that is operable to apply a controllable bias voltage (Vbias) to the gate of the MOS transistor of the cascode stage of each differential side.

22. The power amplifier of claim 13, further comprising a signal level detection and bias determination module that is operable to apply a controllable bias voltage to the gate of the first MOS transistor of each differential side.

23. The power amplifier of claim 13, further comprising a signal level detection and bias determination module that is operable to apply a controllable bias voltage to the gate of the second MOS transistor of each differential side.

24. The power amplifier of claim 13, the transconductance stage of each differential side comprises:

a primary portion that receives the input voltage signal and that produces a primary output current signal;

a secondary portion that receives the input voltage signal and that produces a secondary output current signal; and

wherein the primary output current signal combines with the secondary output current signal to produce the output current signal.

25. The power amplifier of claim 24, wherein the primary portion and the secondary portion of the transconductance stage of each differential side are operable to be biased at different levels.

26. A power amplifier comprising:

a primary cascode amplifier that receives an input voltage signal and that produces a primary current output;

a secondary cascode amplifier that receives the input voltage signal and that produces a secondary current output that is additive to the primary current output;

wherein each of the primary cascode amplifier and the secondary cascode amplifier includes:

a first Metal Oxide Silicon (MOS) transistor having a first gate oxide thickness and a first channel length and a second MOS transistor having a second gate oxide thickness and a second channel length coupled in cascode with the first MOS transistor; and

wherein the second gate oxide thickness is substantially thicker than the first gate oxide thickness.

27. The power amplifier of claim 26, wherein the second gate oxide thickness is approximately twice as thick as the first gate oxide thickness.

28. The power amplifier of claim 27, wherein:

the second gate oxide thickness is approximately 100 Angstroms; and

the first gate oxide thickness is approximately 50 Angstroms.

29. The power amplifier of claim 26, wherein the second channel length is substantially longer than the first channel length.

30. The power amplifier of claim 29, wherein the second channel length is approximately twice as long as the first channel length.

31. The power amplifier of claim 30, wherein:

the second channel length is approximately 0.35 microns; and

the first channel length is approximately 0.18 microns.

32. The power amplifier of claim 26, further comprising a signal level detection and bias determination module that is operable to apply a controllable bias voltage to the gate of the first MOS transistor.

33. The power amplifier of claim 26, further comprising a signal level detection and bias determination module that is operable to apply a controllable bias voltage to the gate of the second MOS transistor.

34. The power amplifier of claim 26, wherein the primary cascode amplifier and the secondary cascode amplifier form a first half of a differential power amplifier and a second half of the differential power amplifier includes corresponding components.

35. The power amplifier of claim 26, wherein the primary cascode amplifier and the secondary cascode amplifier are operable to be biased at different levels.